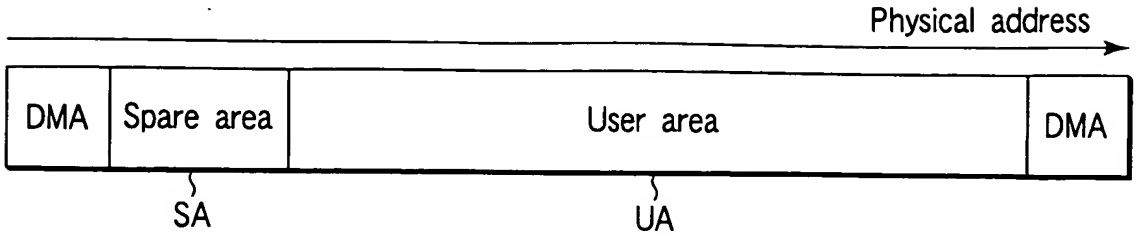

FIG. 1

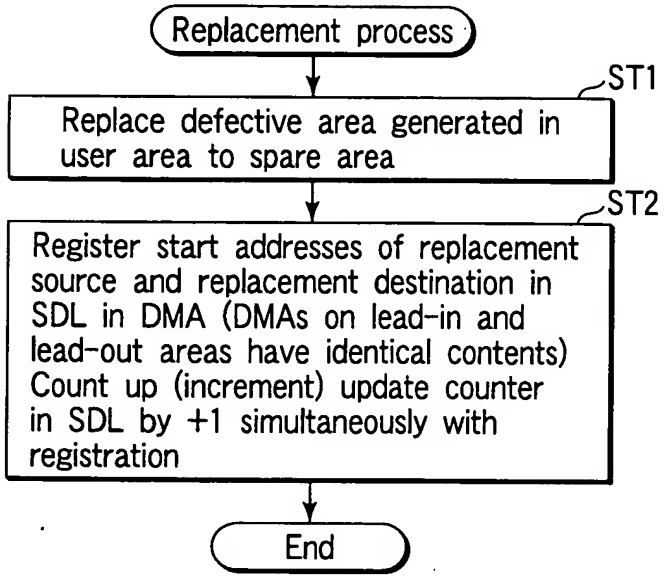

FIG. 2

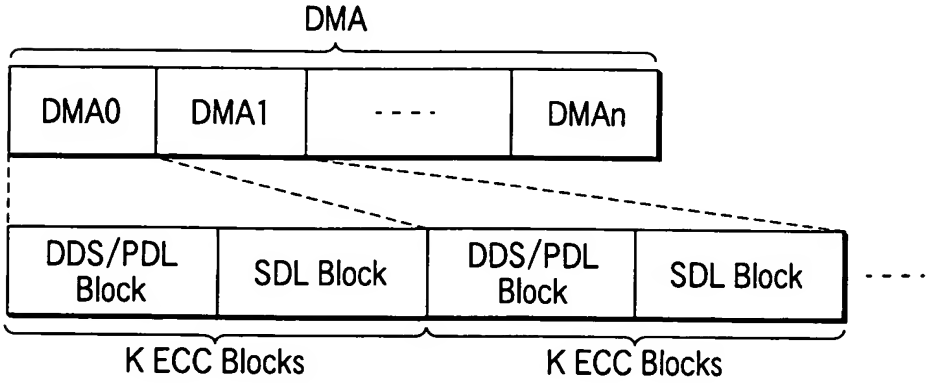

FIG. 3

DDS/PDL

BP	Contents	Number of bytes
0 to 1	DDS identifier (0A0Ah)	2 bytes
2	Reserved	1 byte
3	Disc certification flag	1 byte
4 to 7	DDS/PDL update counter	4 bytes
8 to 9	Number of Groups	2 bytes
10 to 11	Number of zones	2 bytes
12 to 79	Reserved	68 bytes
80 to 87	Location of Primary spare area	8 bytes
88 to 91	Location of LSN 0	4 bytes
92 to 255	Reserved	164 bytes
256 to 259	Start LSN for Zone 0	140 bytes
260 to 263	Start LSN for Zone 1	
.....	.....	
392 to 395	Start LSN for Zone 34	
396 to 399	DMA rec-counter 1	4 bytes
400 to 2047	reserved	1652 bytes

FIG. 4

SDL

BP	Contents	Number of bytes
0 to 1	SDS identifier (0002h)	2 bytes
2 to 3	Reserved	2 bytes
4 to 7	SDL update counter	4 bytes
8 to 11	Start sector number of Supplementary spare area	4 bytes
12 to 15	Total number of logical sectors	4 bytes
16 to 19	DDS/PDL update counter	4 bytes
20	Spare area full flags	1 byte
21 to 24	DMA rec-counter 2	4 bytes
25 to 26	Number of entries in SDL	2 bytes
27 to 34	The first SDL entry	8 bytes
.....	.....	.....
M to m+7	The last SDL entry	8 bytes

FIG. 5

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INV: Hideki TAKAHASHI
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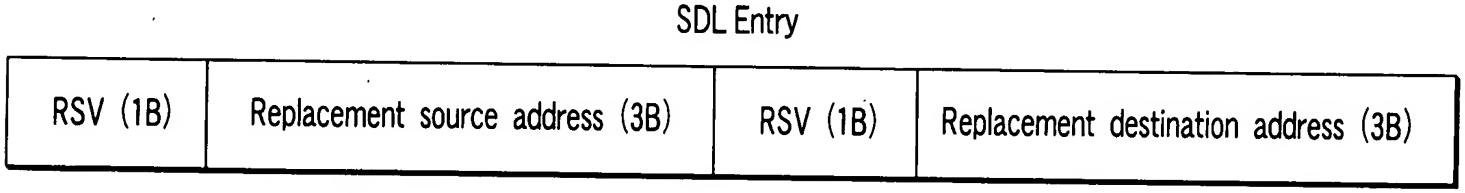

FIG. 6

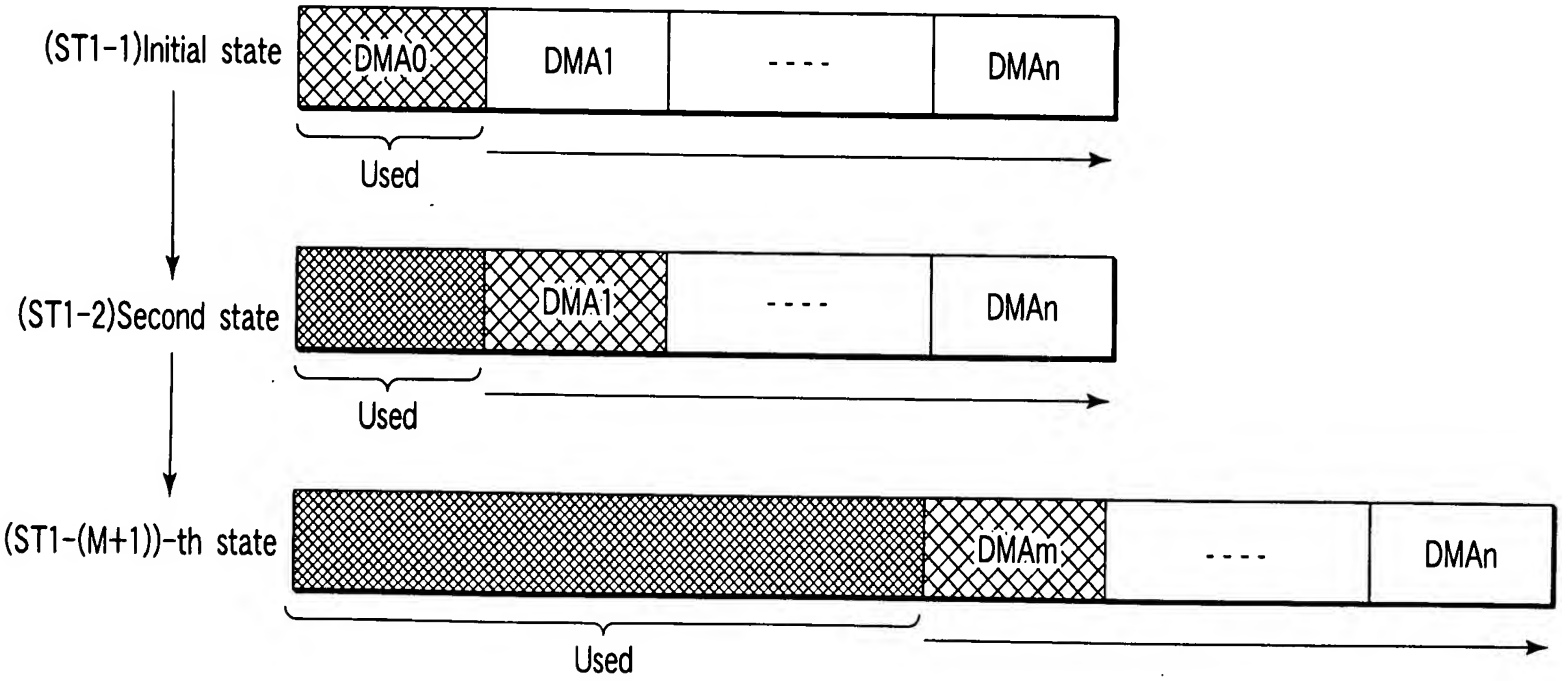

FIG. 7

DMA use state 1

	DDS/PDL update counter	SDL update counter	DMA counter
DMA 0	Normal use	Normal use	0~Nov-1
DMA 1	Continuing use of above value	Continuing use of above value	0~Nov-1
⋮	Continuing use of above value	Continuing use of above value	0~Nov-1
DMA m	Continuing use of above value	Continuing use of above value	0~Nov-1
⋮	Continuing use of above value	Continuing use of above value	0~Nov-1
DMA n	Continuing use of above value	Continuing use of above value	0~Nov-1

Nov : Allowable overwrite count

FIG. 8

DMA use state 2

	DDS/PDL update counter	SDL update counter	DMA counter
DMA 0	Normal use	Normal use	0~Nov-1
DMA 1	Normal use after reset	Normal use after reset	0~Nov-1
⋮	Normal use after reset	Normal use after reset	0~Nov-1
DMA m	Normal use after reset	Normal use after reset	0~Nov-1
⋮	Normal use after reset	Normal use after reset	0~Nov-1
DMA n	Normal use after reset	Normal use after reset	0~Nov-1

Nov : Allowable overwrite count

FIG. 9

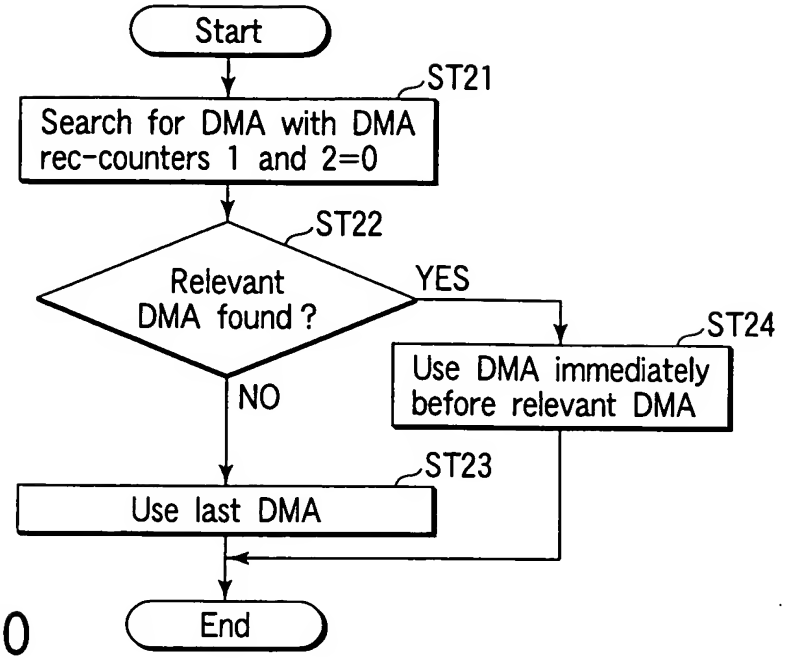
Start
ST21
Search for DMA with DMA rec-counters 1 and 2=0
ST22
Relevant DMA found ?
YES
NO
ST24
Use DMA immediately before relevant DMA
ST23
Use last DMA
End

FIG. 10

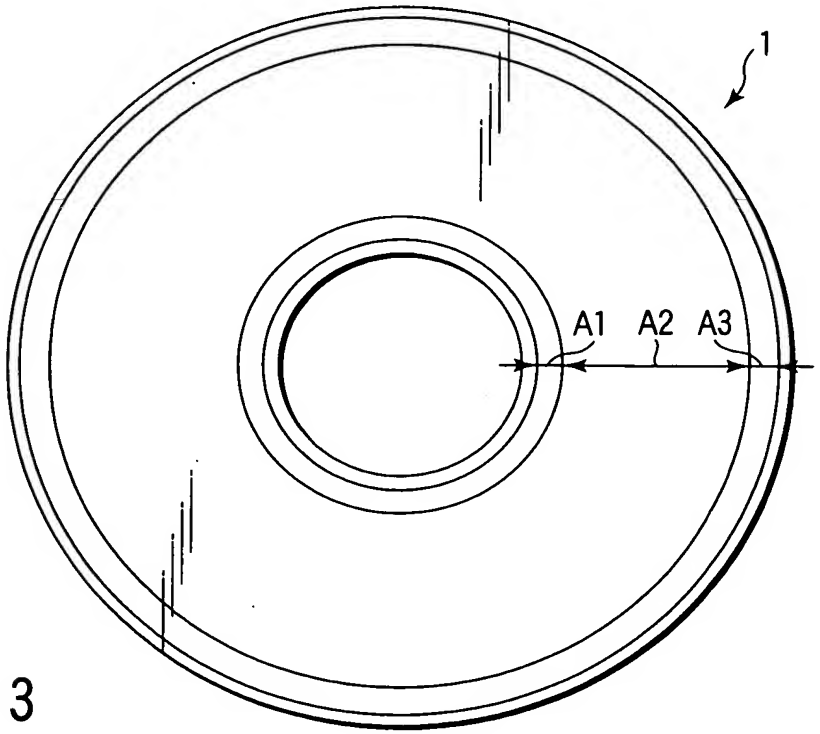
1
A1
A2
A3

FIG. 13

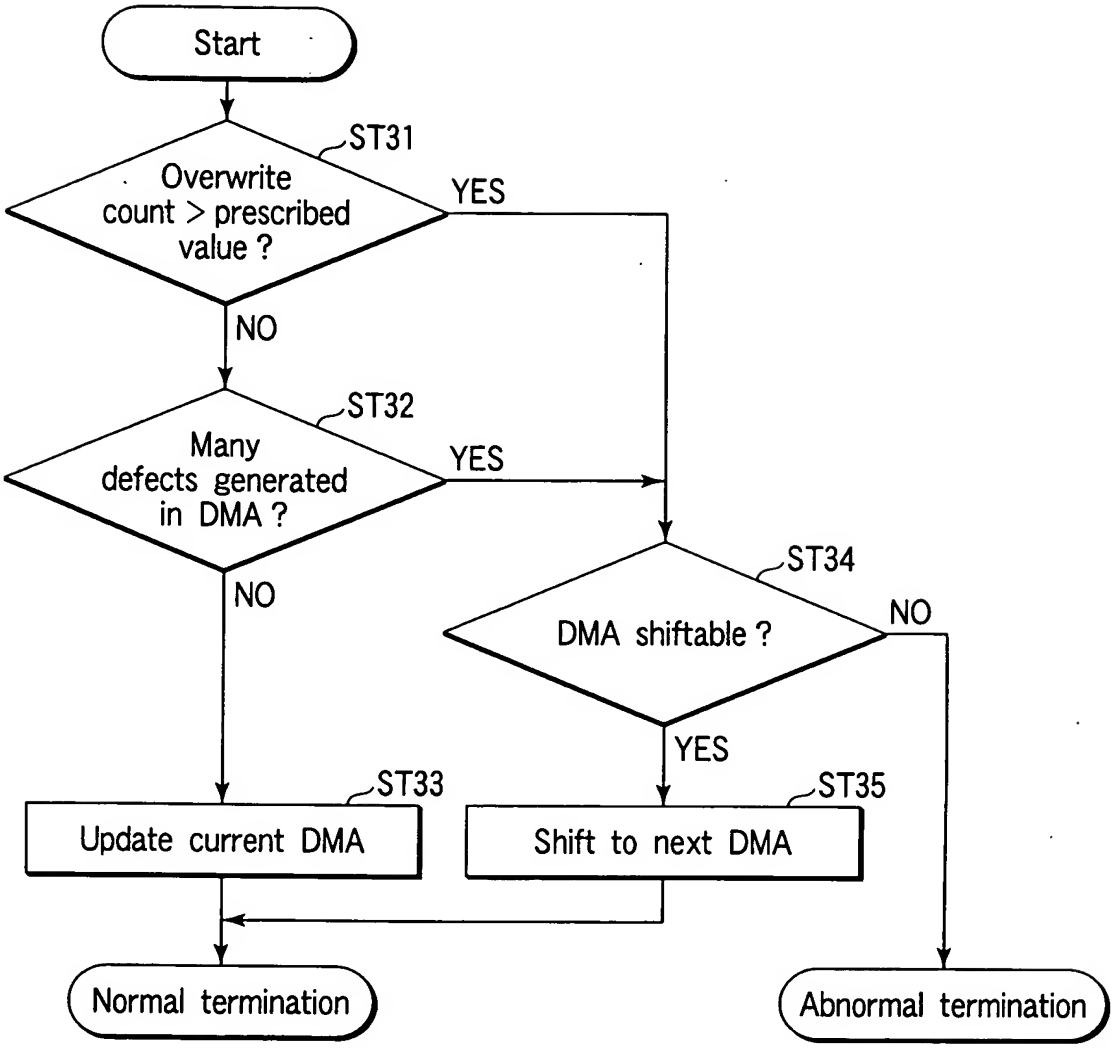
Start
ST31
Overwrite count > prescribed value ?
YES
NO
ST32
Many defects generated in DMA ?
YES
NO
ST34
DMA shiftable ?
NO
YES
ST33
Update current DMA
ST35
Shift to next DMA
Normal termination
Abnormal termination

FIG. 11

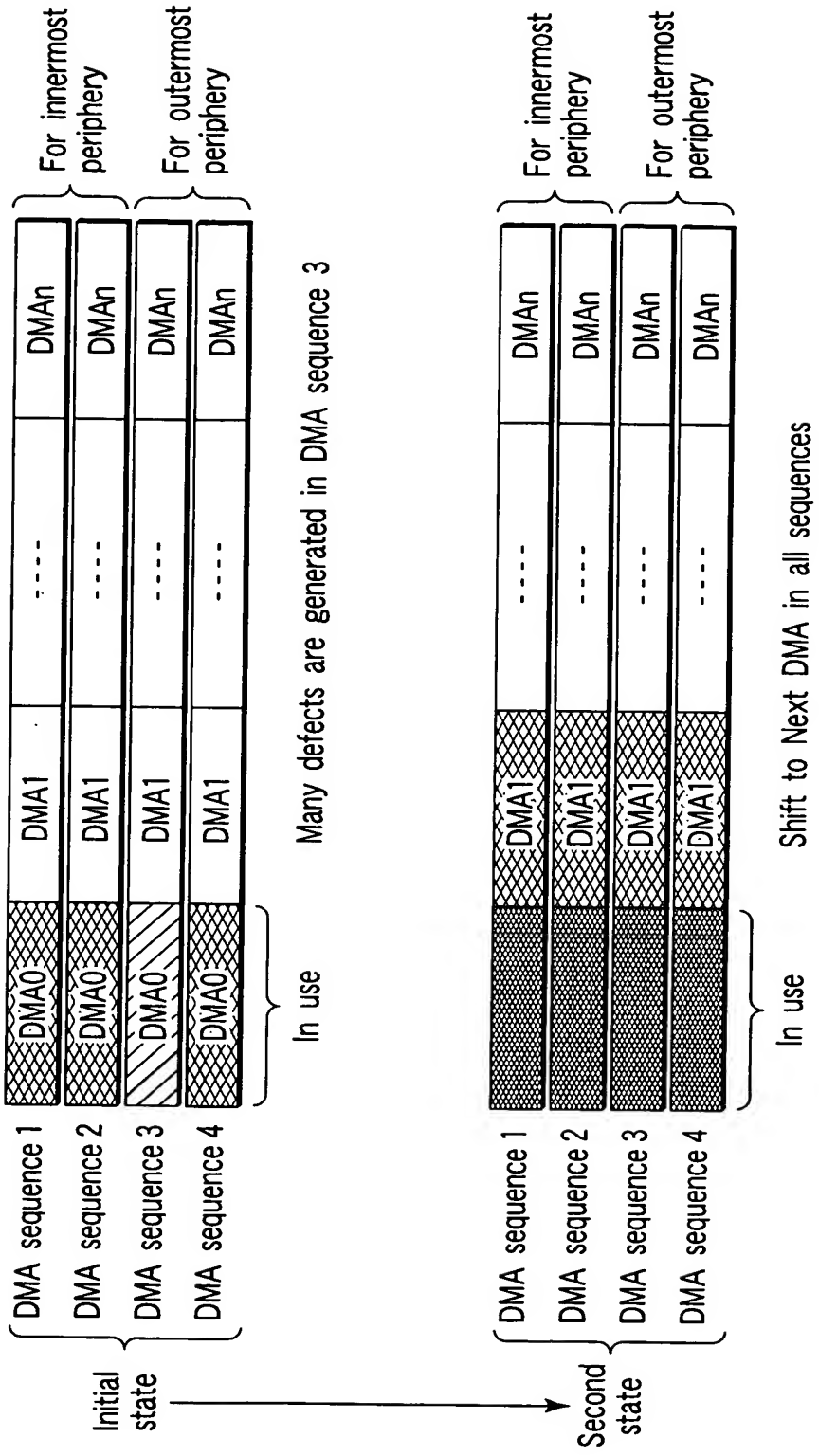
Initial state
Second state
DMA sequence 1
DMA sequence 2
DMA sequence 3
DMA sequence 4
DMA0
DMA1
DMAn
For innermost periphery
For outermost periphery
In use
Many defects are generated in DMA sequence 3
Shift to Next DMA in all sequences

FIG. 12

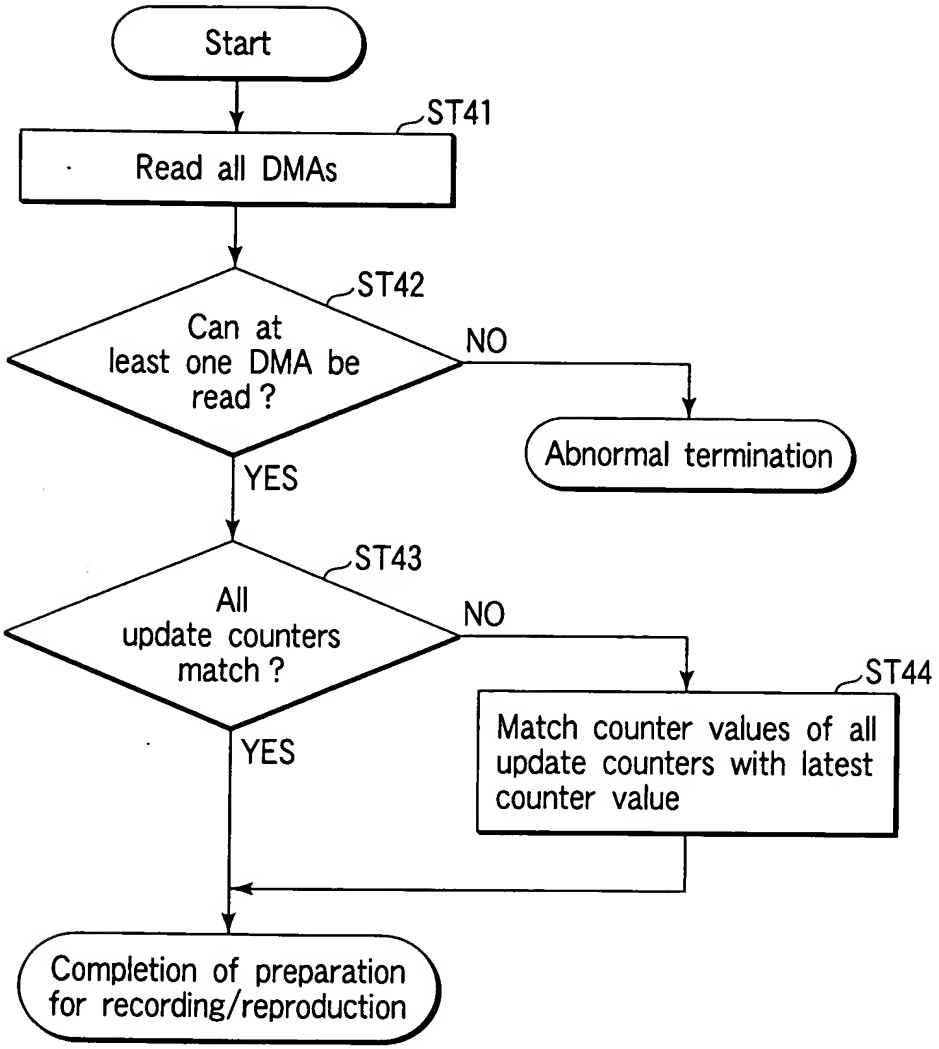
Start
ST41
Read all DMAs
ST42
Can at least one DMA be read ?
NO
Abnormal termination
YES
ST43
All update counters match ?
NO
ST44
Match counter values of all update counters with latest counter value
YES
Completion of preparation for recording/reproduction

FIG. 14

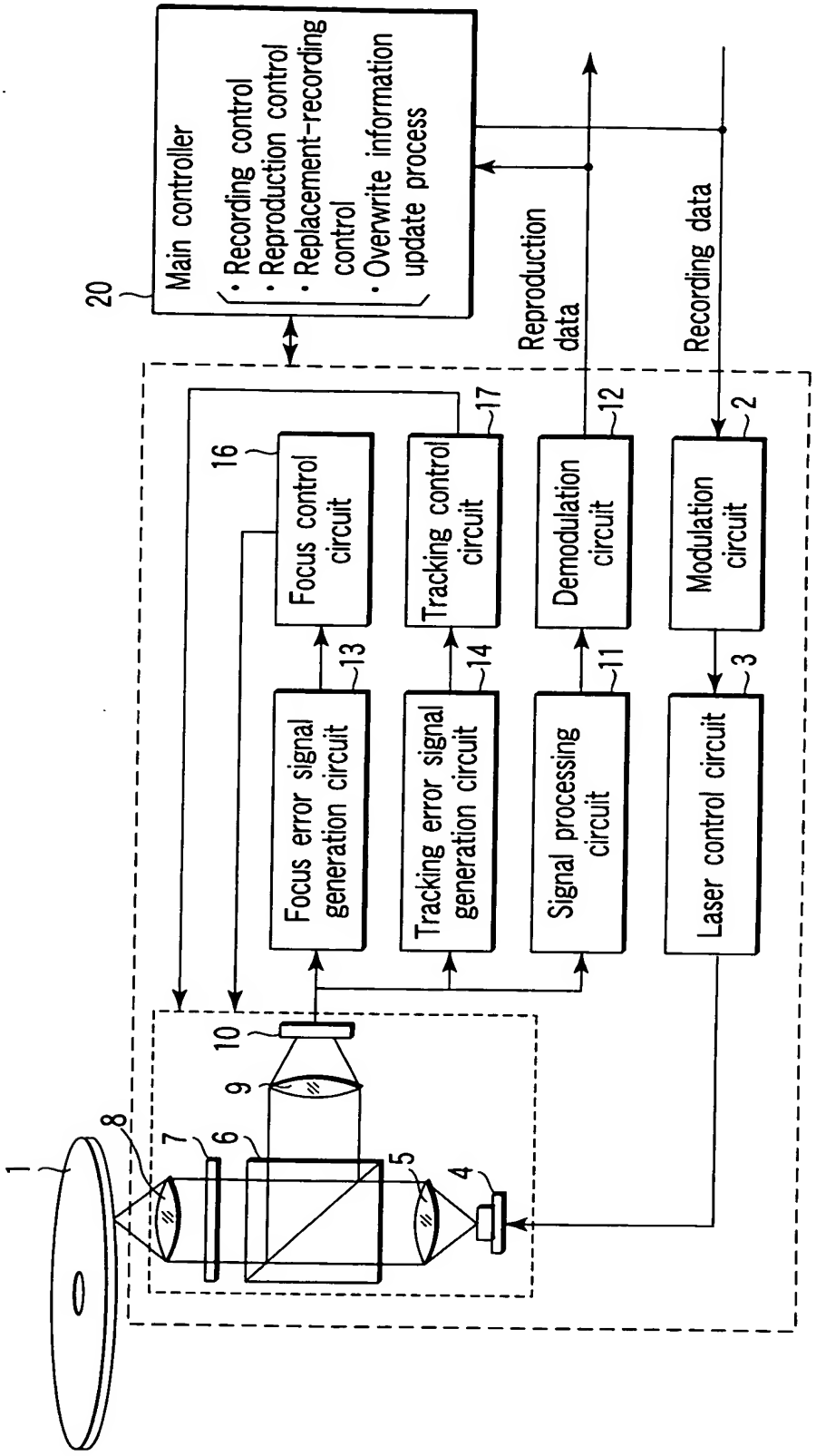
20
Main controller
• Recording control
• Reproduction control
• Replacement-recording control
• Overwrite information update process
Reproduction data
Recording data
16
Focus control circuit
17
Tracking control circuit
12
Demodulation circuit
2
Modulation circuit
13
Focus error signal generation circuit
14
Tracking error signal generation circuit
11
Signal processing circuit
3
Laser control circuit
10
9
8
7
6
5
4
1

FIG. 15

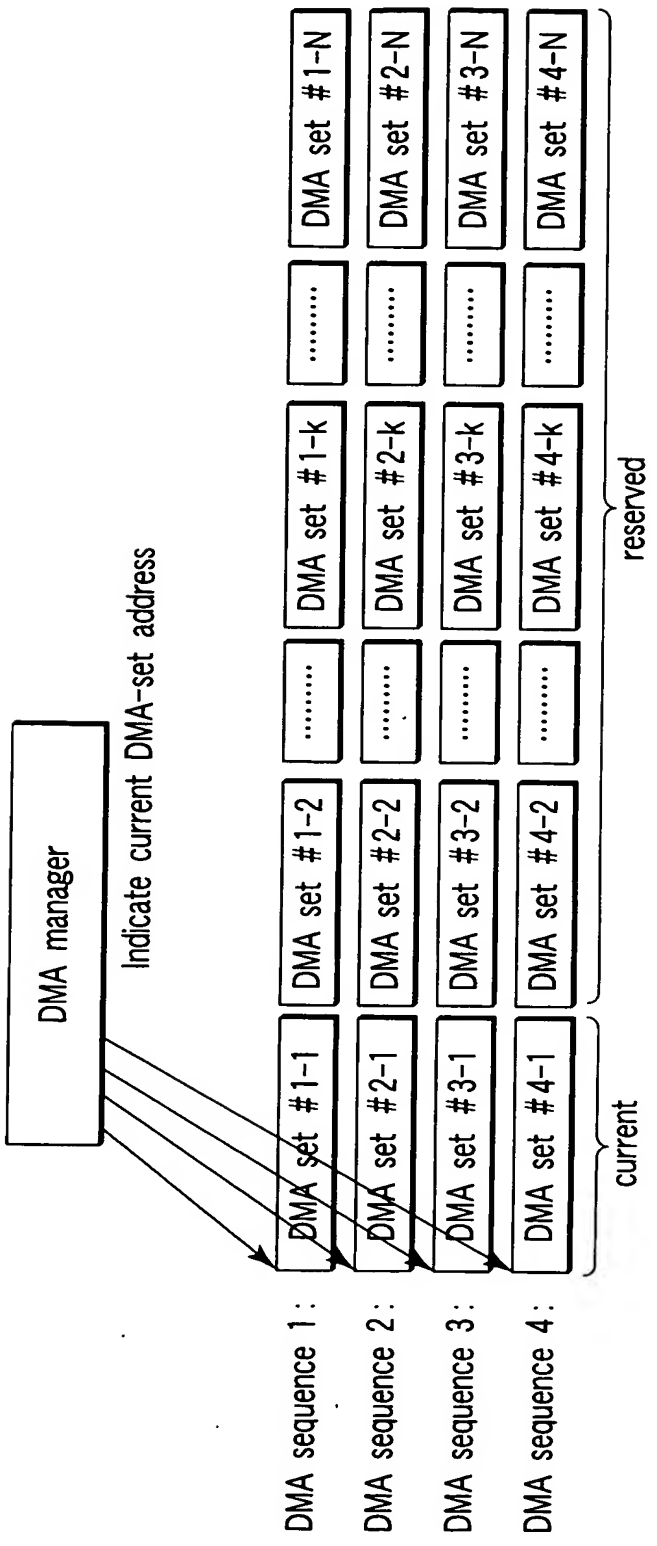
DMA manager
Indicate current DMA-set address
DMA sequence 1 :
DMA sequence 2 :
DMA sequence 3 :
DMA sequence 4 :
DMA set #1-1
DMA set #1-2
DMA set #1-k
DMA set #1-N
DMA set #2-1
DMA set #2-2
DMA set #2-k
DMA set #2-N
DMA set #3-1
DMA set #3-2
DMA set #3-k
DMA set #3-N
DMA set #4-1
DMA set #4-2
DMA set #4-k
DMA set #4-N
current
reserved

FIG. 16

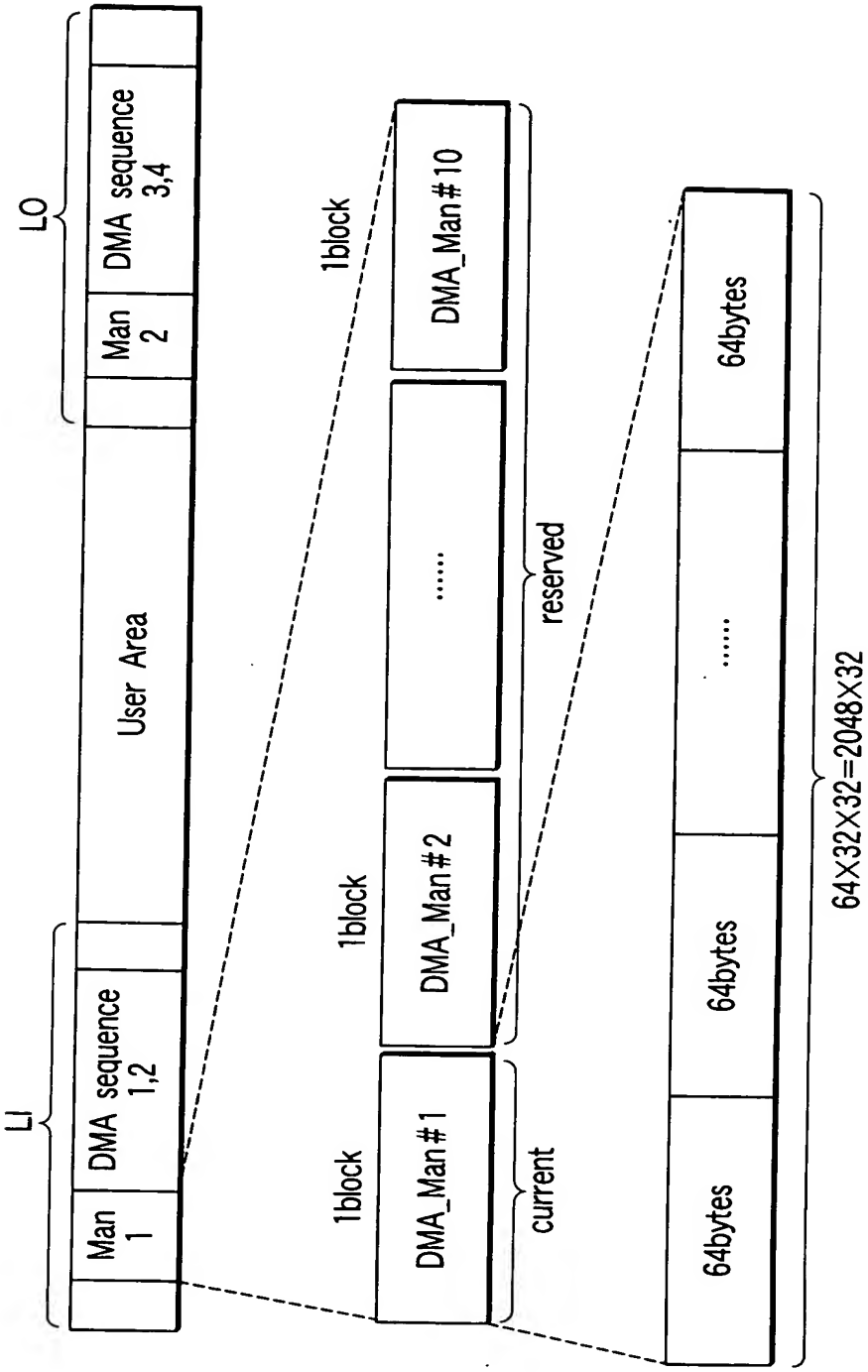
LI
Man 1
DMA sequence 1,2
User Area
LO
Man 2
DMA sequence 3,4
1block
DMA_Man#1
current
1block
DMA_Man#2
.....
1block
DMA_Man#10
reserved
64bytes
64bytes
.....
64bytes
64X32X32=2048X32
Redundant data against defect
Each 64bytes is identical.

FIG. 17

BP	Contents	Number of bytes
0 to 1	Identifier (0010h)	2bytes
2 to 7	Reserved	6bytes
8 to 11	First PSN of current DMA sequence 1	4bytes
12 to 15	First PSN of current DMA sequence 2	4bytes
16 to 19	First PSN of current DMA sequence 3	4bytes
20 to 23	First PSN of current DMA sequence 4	4bytes
24 to 63	Reserved	40bytes

FIG. 18

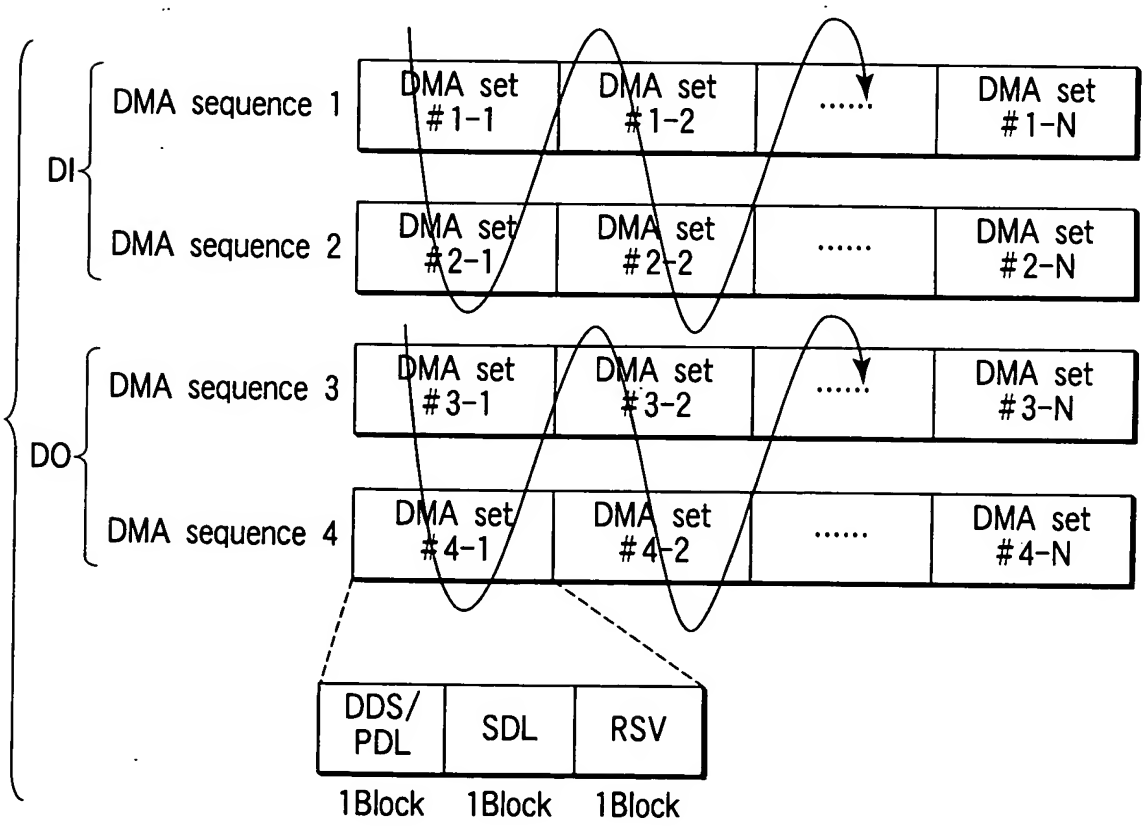

FIG. 19

Each DMA	2Blocks (DDS/PDL block and SDL block)
DMA set	300Blocks=100set
Number of DMA set	4Blocks (LI : 2, LO : 2)
Total Blocks for DMA	1200Blocks (300blocks * 4set)
Each DMA Manager	1Block
Number of DMA Manager	10Blocks

FIG. 20

	Normal	Abnormal	
Defective DMA	Defective	Not Defective (Readable)	Blank
Current DMA	Not Defective (Readable)	Defective	Blank
Reserved DMA	Blank	–	

FIG. 24

Case	head	body	tail	Comment
1	Reserved	Reserved	Reserved	Unformatted
2	Current	Reserved	Reserved	Initial
3	Defect	Current	Reserved	
4	Defect	Defect	Current	Last
5	Defect	Defect	Defect	All defect

FIG. 25

Lead-in		Start Physical sector number	END Physical sector number	Number of Blocks	Lead-out		Start Physical sector number	END Physical sector number	Number of Blocks
	DMA Manager1-1	2CE00	2CE1F	1		DMA Manager2-1	4ED740	4ED75F	1
	reserved	2CE20	2CE5F	2		reserved	4ED760	4ED79F	2
	DMA manager1-2	2CE60	2CE7F	1		DMA manager2-2	4ED7A0	4ED7BF	1
	reserved	2CE80	2CEBF	2		reserved	4ED7C0	4ED7FF	2
	.....					.....			
	DMA manager1-10	2D160	2D17F	1		DMA manager2-10	4EDAA0	4EDABF	1
	reserved	2D180	2D1BF	2		reserved	4EDAC0	4EDAFF	2
	DMA1-1	2D1C0	2D1FF	2		DMA3-1	4EDB00	4EDB3F	2
	reserved	2D200	2D21F	1		reserved	4EDB40	4EDB5F	1
	DMA2-1	2D220	2D25F	2		DMA4-1	4EDB60	4EDB9F	2
	reserved	2D260	2D27F	1		reserved	4EDBA0	4EDBBF	1
	DMA1-2	2D280	2D2BF	2		DMA3-2	4EDBC0	4EDBFF	2
	reserved	2D2C0	2D2DF	1		reserved	4EDC00	4EDC1F	1
	DMA2-2	2D2E0	2D31F	2		DMA4-2	4EDC20	4EDC5F	2
	reserved	2D320	2D33F	1		reserved	4EDC60	4EDC7F	1
	.....					.....			
	DMA1-48	2F500	2F53F	2		DMA3-48	4EFE40	4EFE7F	2
	reserved	2F540	2F55F	1		reserved	4EFE80	4EFE9F	1
	DMA2-48	2F560	2F59F	2		DMA4-48	4EFEA0	4EFEDF	2
	reserved	2F5A0	2F5BF	1		reserved	4EFEE0	4EFEFF	1
	DMA1-49	82CE00	82CE3F	2		DMA3-49	CED740	CED77F	2
	reserved	82CE40	82CE5F	1		reserved	CED780	CED79F	1
	DMA2-49	82CE60	82CE9F	2		DMA4-49	CED7A0	CED7DF	2
	reserved	82CEA0	82CEBF	1		reserved	CED7E0	CED7FF	1
	.....					.....			
	DMA1-100	82F440	82F47F	2		DMA3-100	CEFD80	CEFDBF	2
	reserved	82F480	82F49F	1		reserved	CEFDC0	CEFDDF	1
	DMA2-100	82F4A0	82F4DF	2		DMA4-100	CEFDE0	CEFE1F	2
	reserved	82F4E0	82F4FF	1		reserved	CEFE20	CEFE3F	1

FIG. 21

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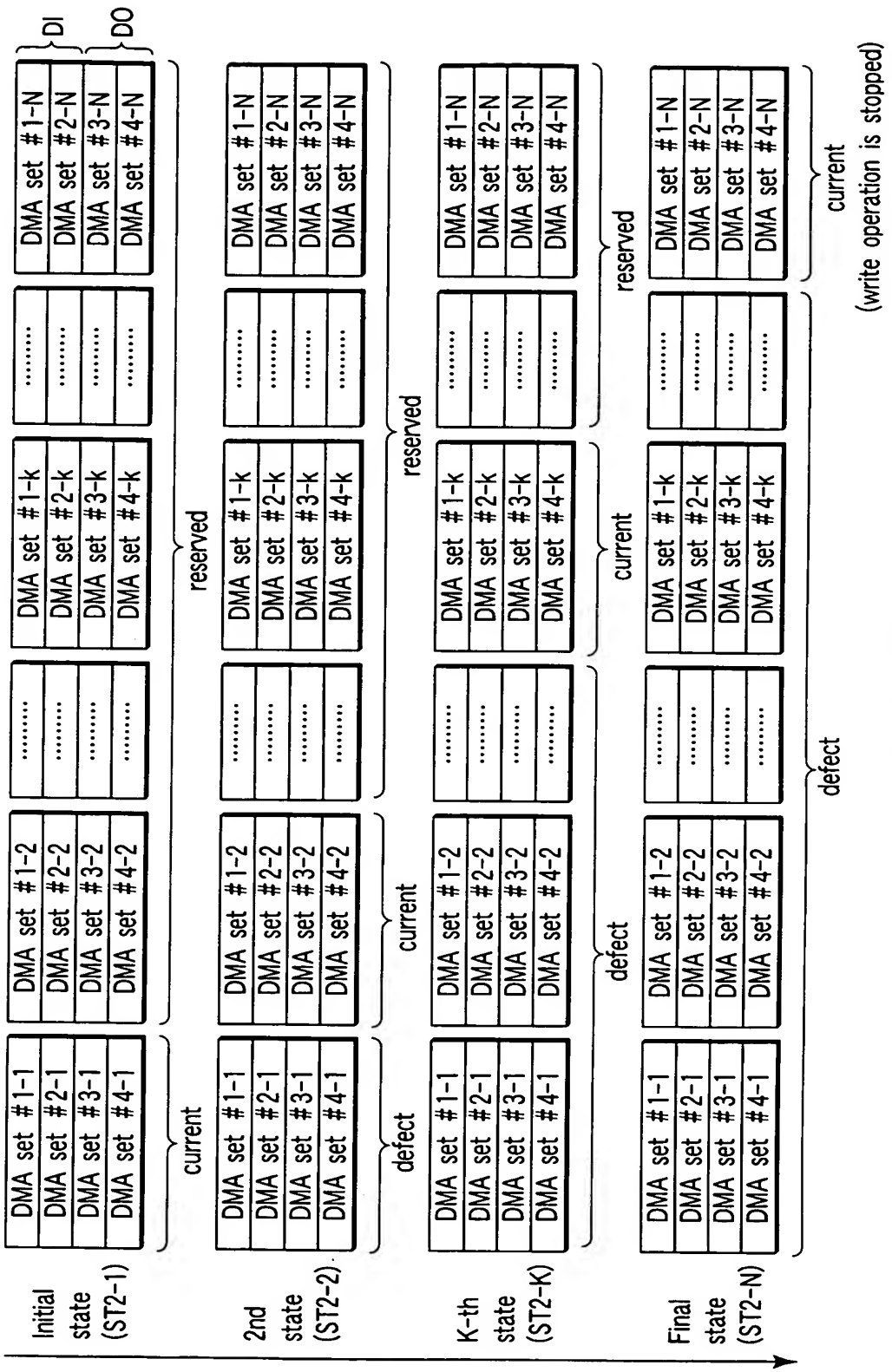
DI
DO
DMA set #1-1
DMA set #2-1
DMA set #3-1
DMA set #4-1
DMA set #1-2
DMA set #2-2
DMA set #3-2
DMA set #4-2
DMA set #1-k
DMA set #2-k
DMA set #3-k
DMA set #4-k
DMA set #1-N
DMA set #2-N
DMA set #3-N
DMA set #4-N
current
reserved
defect
Initial state (ST2-1)
2nd state (ST2-2)
K-th state (ST2-K)
Final state (ST2-N)
(write operation is stopped)

FIG. 22

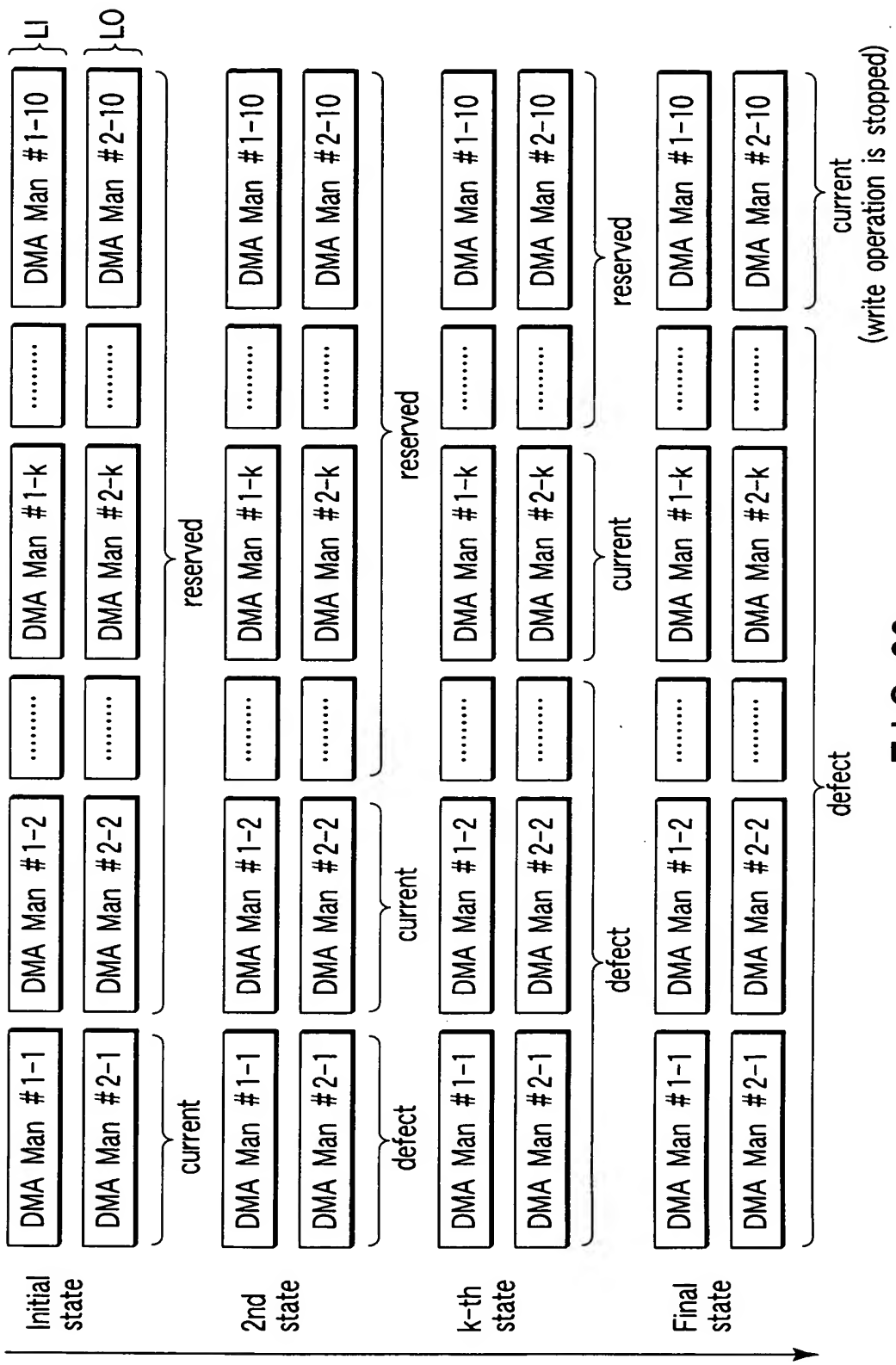
Initial state
2nd state
k-th state
Final state
DMA Man #1-1
DMA Man #2-1
DMA Man #1-2
DMA Man #2-2
DMA Man #1-k
DMA Man #2-k
DMA Man #1-10
DMA Man #2-10
LI
LO
current
defect
reserved
current
reserved
defect
current
reserved
current
(write operation is stopped)
defect

FIG. 23

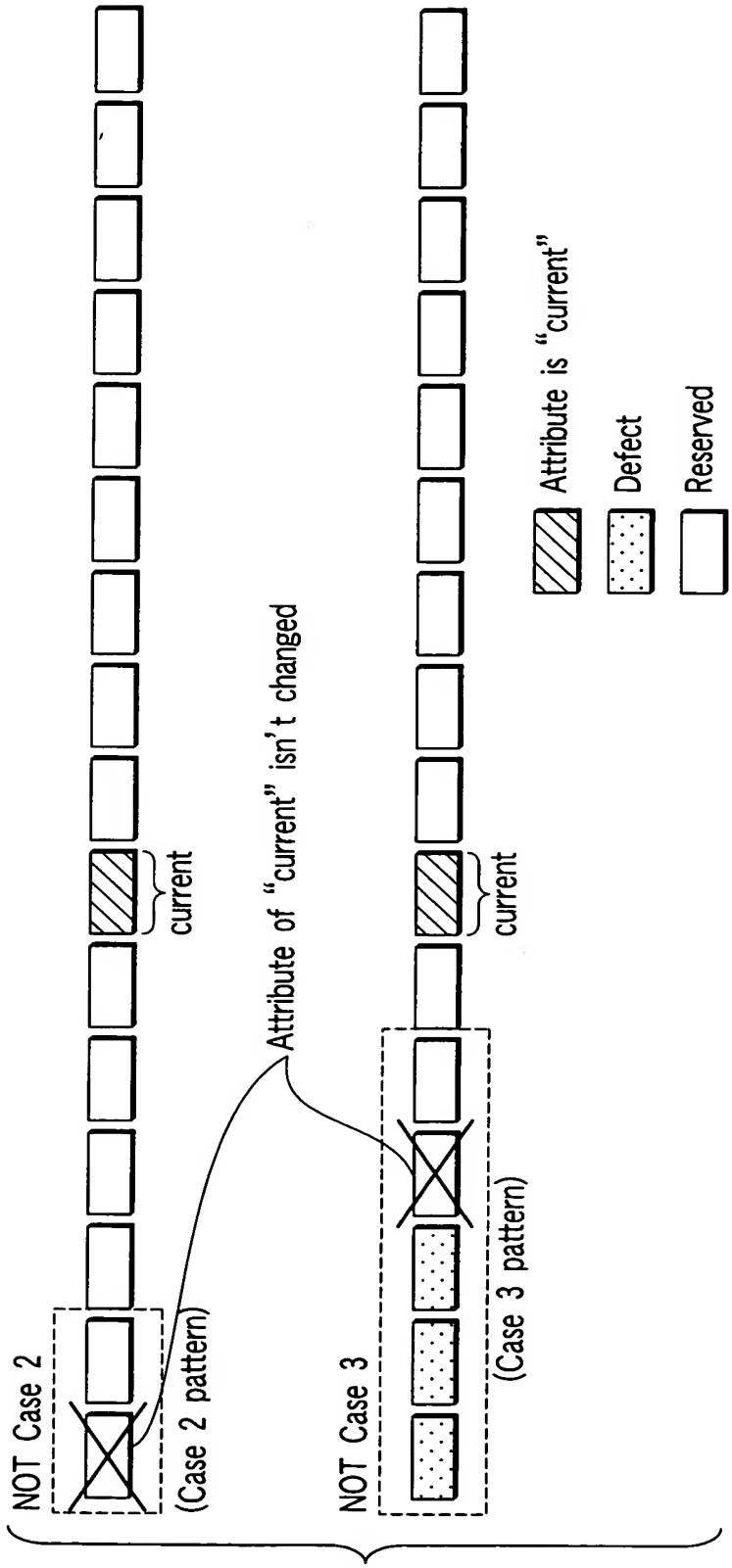
NOT Case 2
(Case 2 pattern)
current
Attribute of "current" isn't changed
NOT Case 3
(Case 3 pattern)
current
Attribute is "current"
Defect
Reserved

FIG. 26

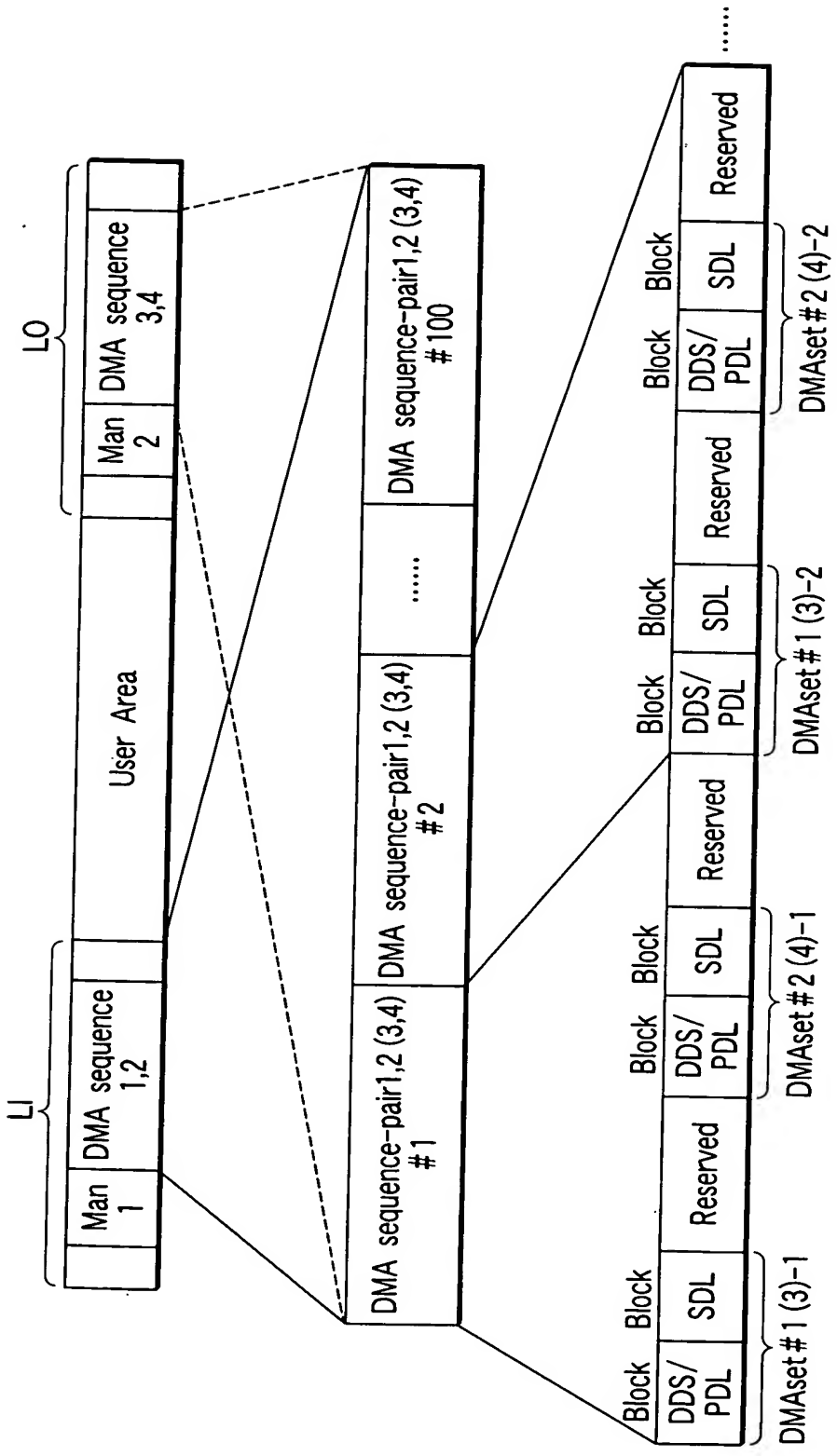
LI
Man 1
DMA sequence 1,2
User Area
LO
Man 2
DMA sequence 3,4
DMA sequence-pair1,2 (3,4) #1
DMA sequence-pair1,2 (3,4) #2
.....
DMA sequence-pair1,2 (3,4) #100
Block
DDS/ PDL
SDL
Reserved
DMAset # 1 (3)-1
DMAset # 2 (4)-1
DMAset # 1 (3)-2
DMAset # 2 (4)-2

FIG. 27

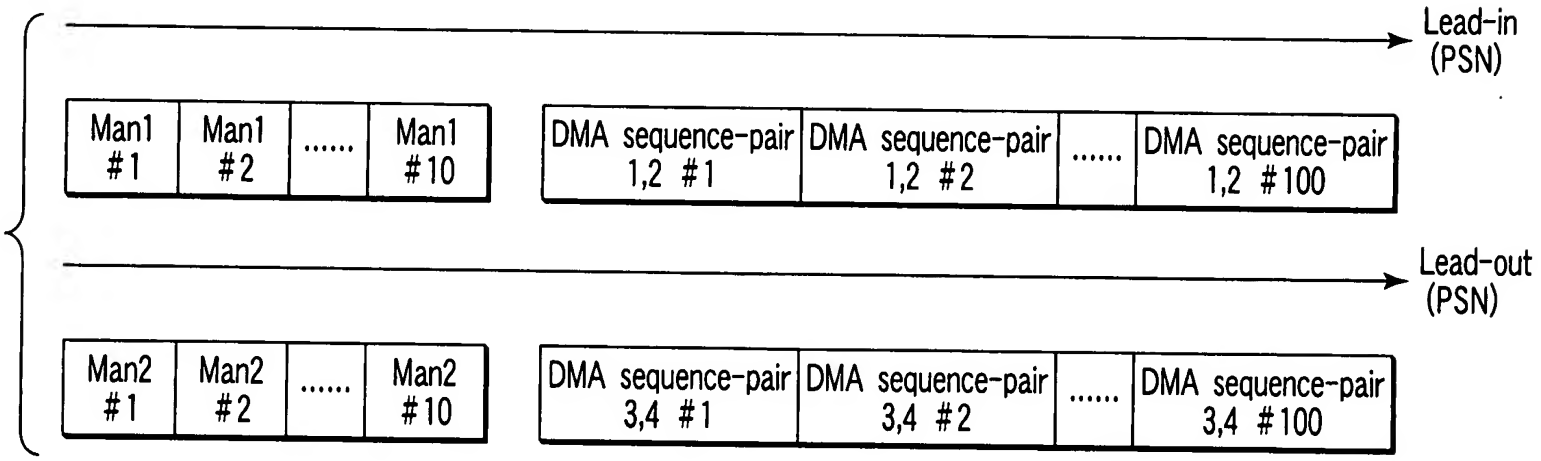

FIG. 28

FIG. 30

BP	Contents	Number of bytes
0 to 1	PDL Identifier (0001h)	2bytes
2 to 3	Number of entries in the PDL (E_{PDL})	2bytes
4 to 7	The first PDL entry	4bytes
8 to 11	The second PDL entry	4bytes
.....	.....	.....
n to n+3	The last PDL entry	4bytes

$n=4*E_{PDL}$

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DOCKET #: 250752US2S
INV: Hideki TAKAHASHI
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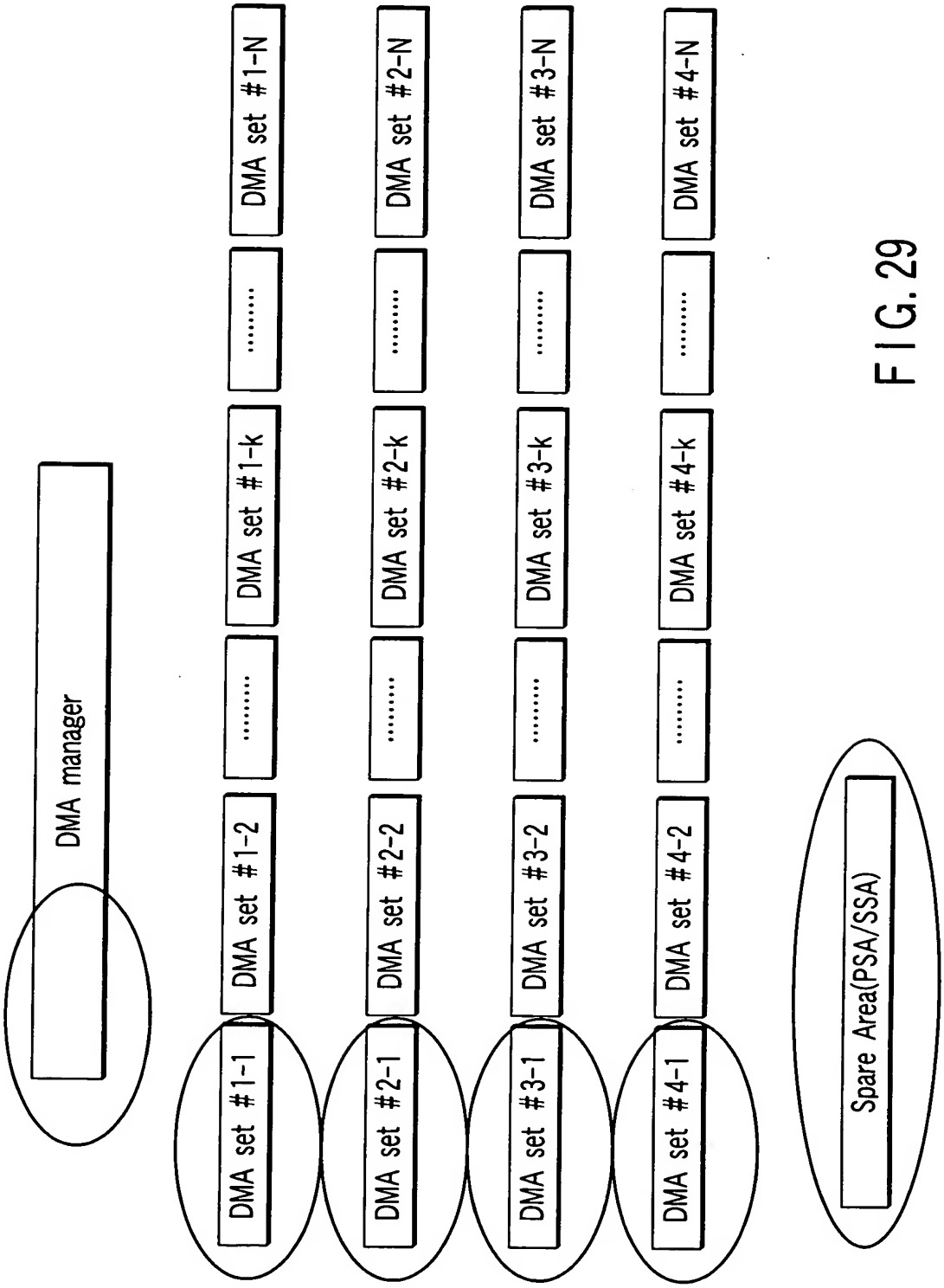

DMA manager
DMA set #1-1
DMA set #1-2
.....
DMA set #1-k
.....
DMA set #1-N
DMA set #2-1
DMA set #2-2
.....
DMA set #2-k
.....
DMA set #2-N
DMA set #3-1
DMA set #3-2
.....
DMA set #3-k
.....
DMA set #3-N
DMA set #4-1
DMA set #4-2
.....
DMA set #4-k
.....
DMA set #4-N
Spare Area(PSA/SSA)

FIG. 29

BP	Contents	Number of bytes
0 to 1	SDL Identifier (0002h)	2bytes
2 to 3	Reserved	2bytes
4 to 7	SDL update counter	4bytes
8 to 11	Start sector number of Supplementary spare area	4bytes
12 to 15	Total number of logical sectors	4bytes
16 to 19	DDS/PDL update counter	4bytes
20	Spare area full flags	1byte
21	Reserved	1byte
22 to 23	Number of entries in SDL (E_{SDL})	2bytes
24 to 31	The first SDL entry	8bytes
.....	.....	.....
m to m+7	The last SDL entry	8bytes

$m=8*E_{SDL}+16$

FIG. 31

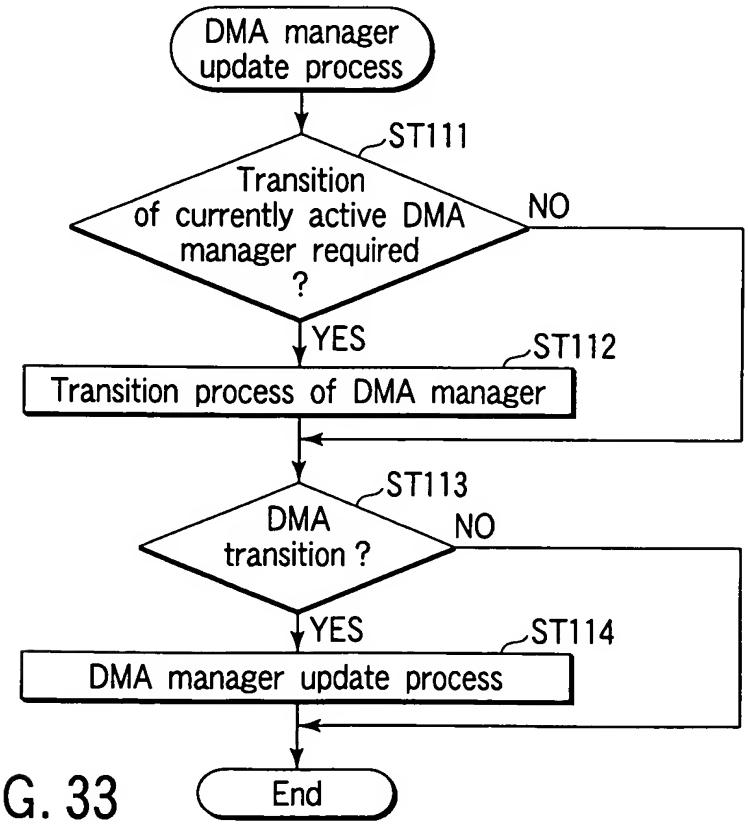


FIG. 33

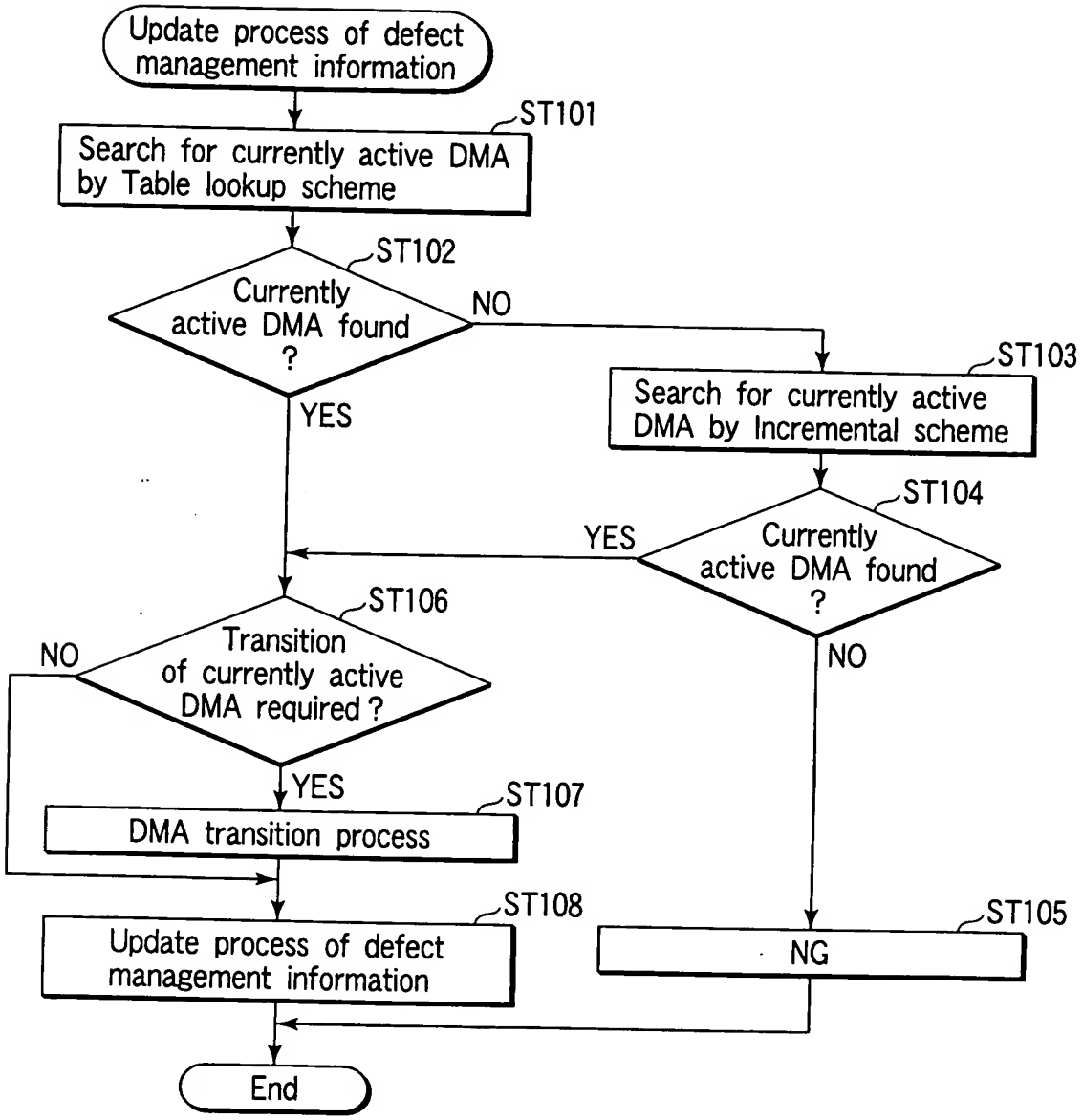

Update process of defect management information
ST101
Search for currently active DMA by Table lookup scheme
ST102
Currently active DMA found ?
NO
YES
ST103
Search for currently active DMA by Incremental scheme
ST104
Currently active DMA found ?
YES
NO
ST106
Transition of currently active DMA required ?
NO
YES
ST107
DMA transition process
ST108
Update process of defect management information
ST105
NG
End

FIG. 32

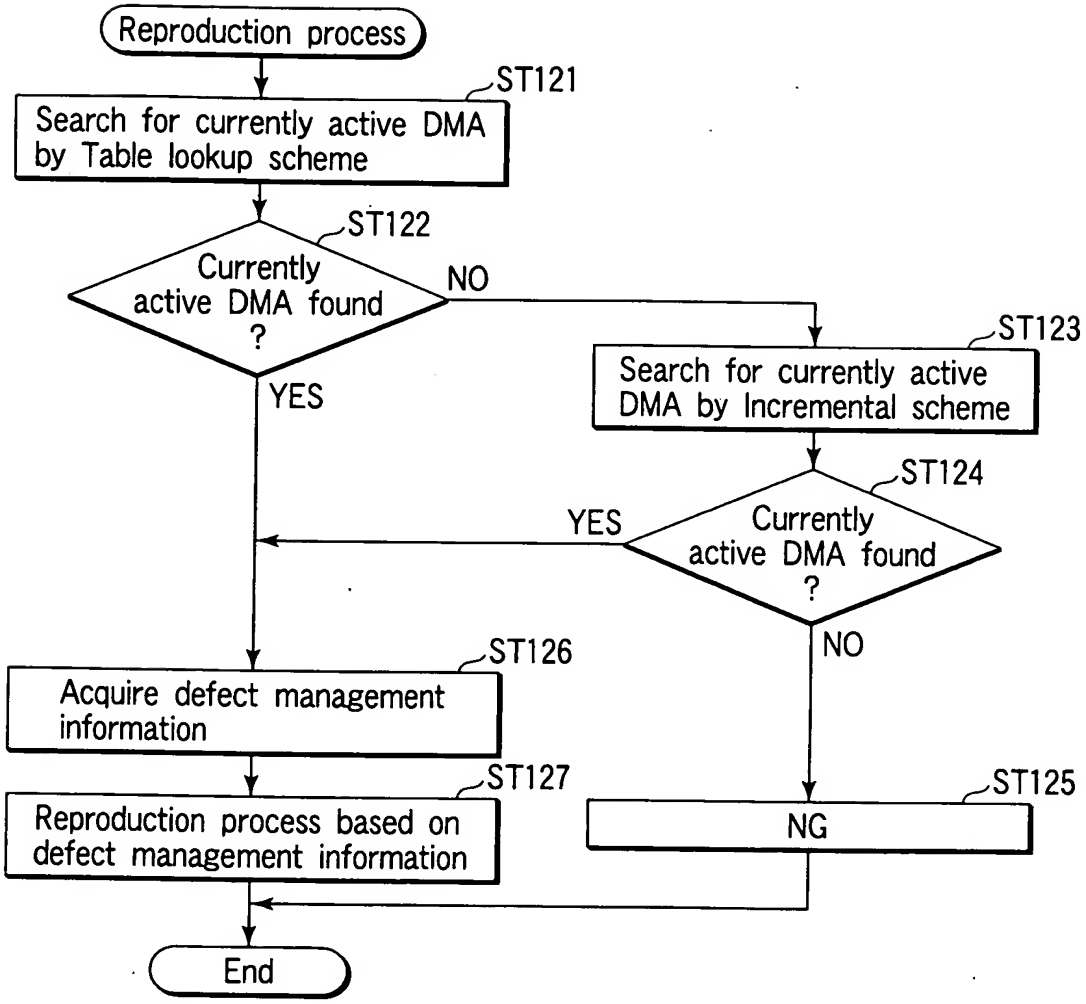
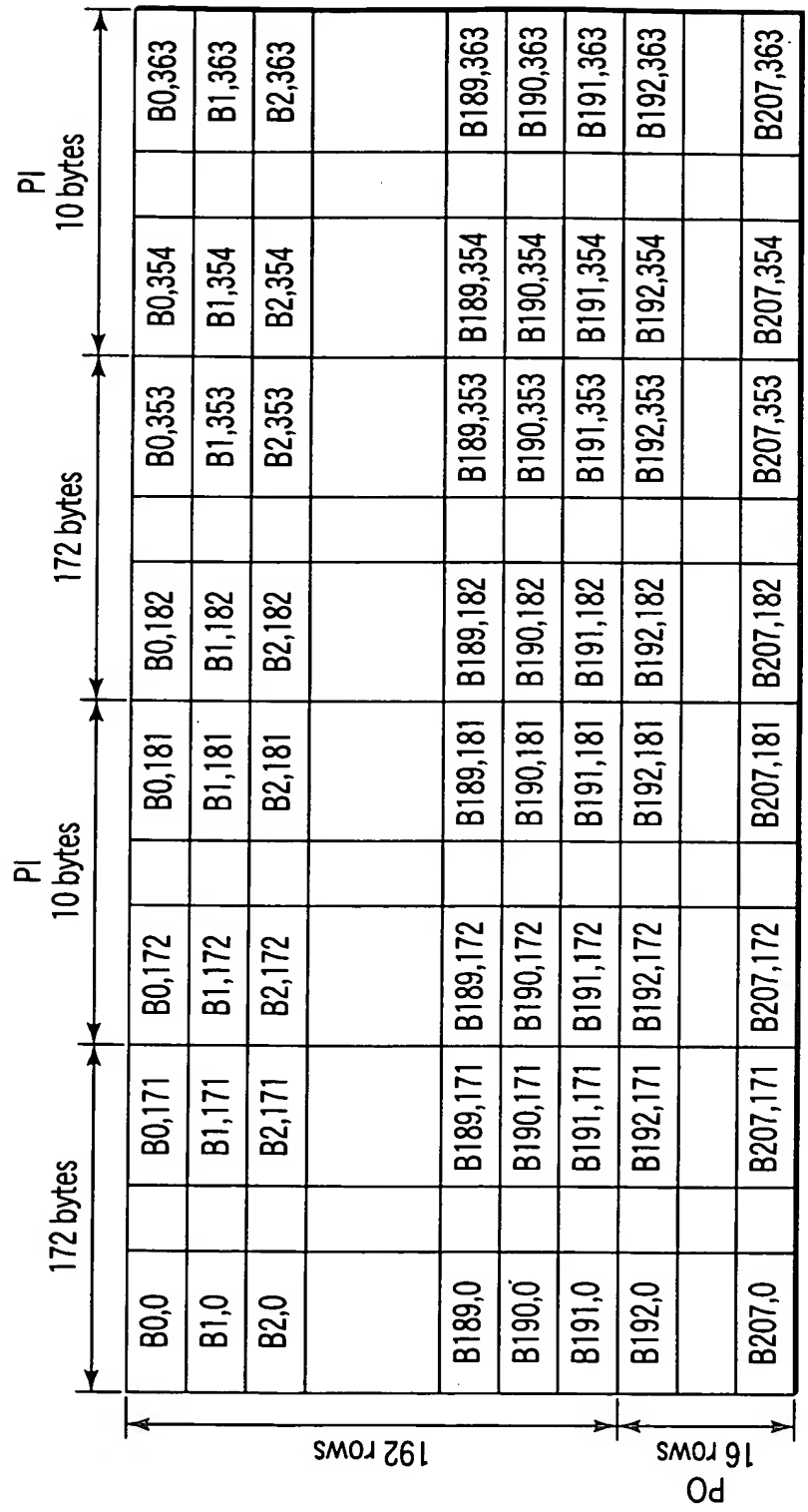

Reproduction process
ST121
Search for currently active DMA by Table lookup scheme
ST122
Currently active DMA found ?
NO
YES
ST123
Search for currently active DMA by Incremental scheme
ST124
YES
Currently active DMA found ?
NO
ST126
Acquire defect management information
ST127
Reproduction process based on defect management information
ST125
NG
End

FIG. 34



(ECC block structure (D, E))

FIG. 35

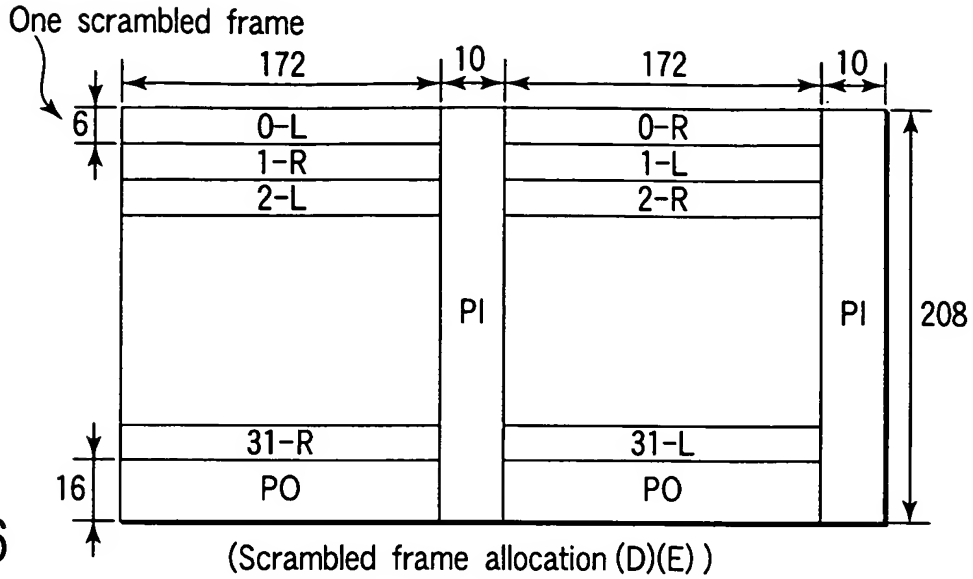


FIG. 36

(Scrambled frame allocation (D)(E))

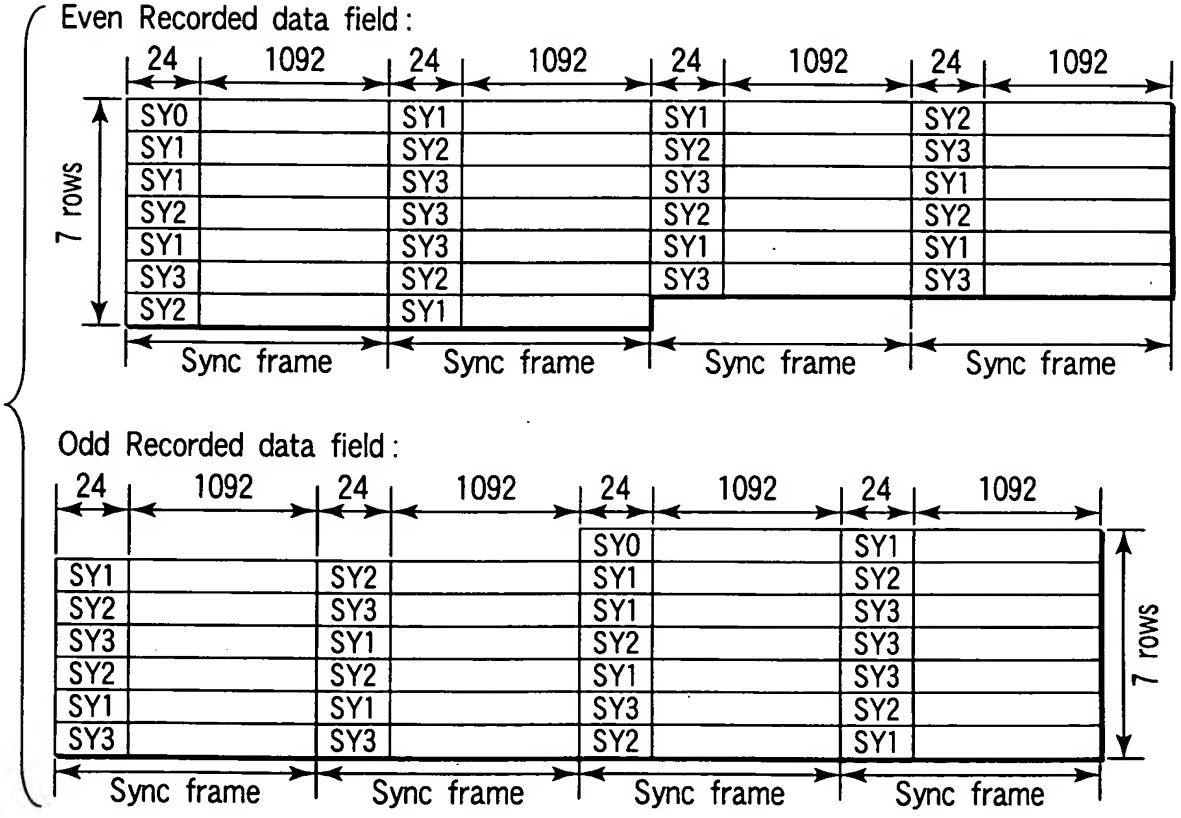


FIG. 38

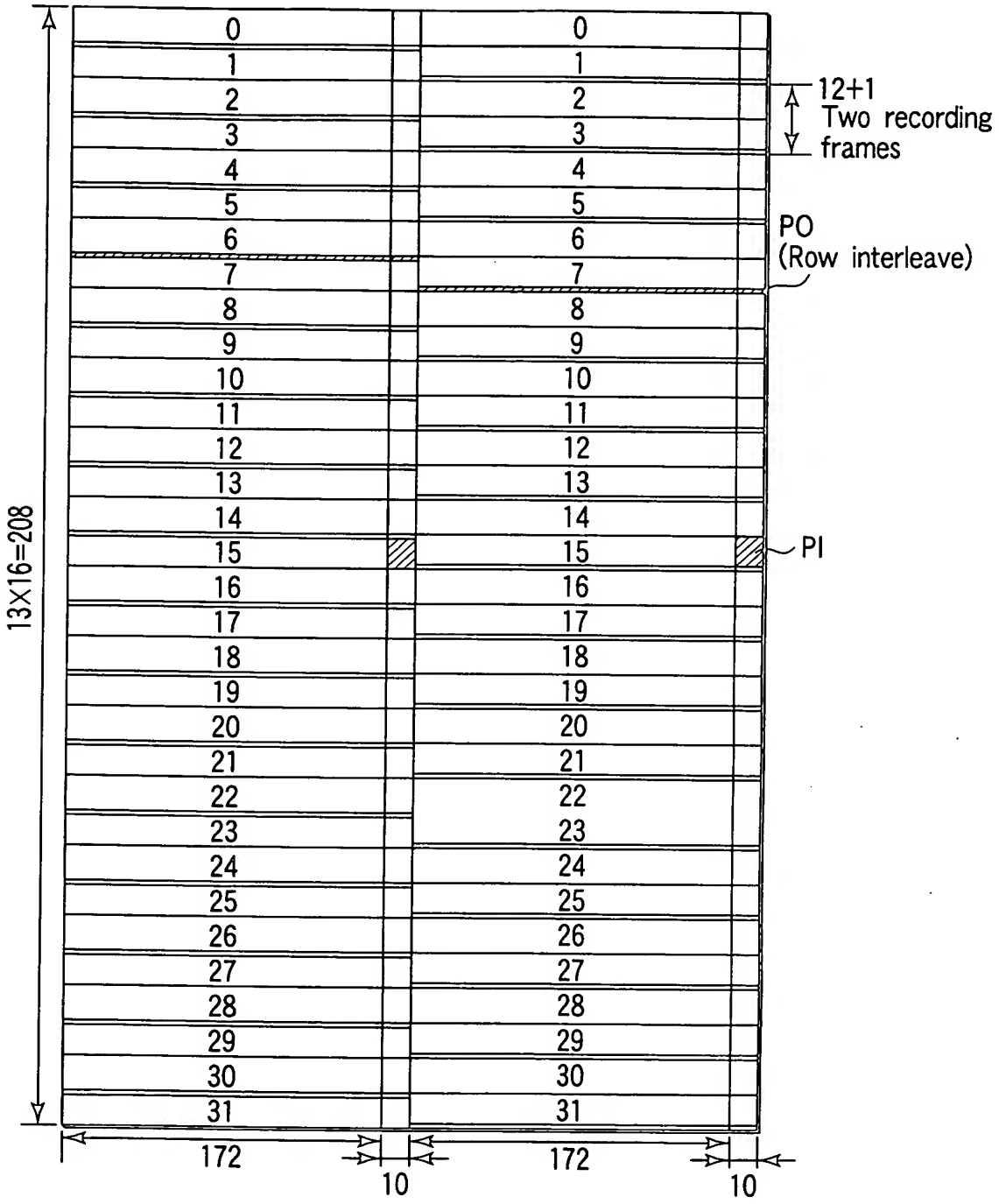

0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
12+1
Two recording
frames
PO
(Row interleave)
PI
13X16=208
172
10
172
10

FIG. 37